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09/927,042	08/09/2001	John K. Walton	EMC-01-017	4723

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EXAMINER	
DILDINE JR, R STEPHEN	

ART UNIT	PAPER NUMBER
2133	4

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	09/927,042	WALTON ET AL.
	Examiner	Art Unit
	R. Stephen Dildine	2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-20 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1,2,4-12 and 14-20 is/are rejected.

7)☒ Claim(s) 3 and 13 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 August 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Specification

The disclosure is objected to because of the following informalities: At page 14, line 3; "Application Serial No. 09/745,814" should be updated to -- No. 6,636,933 --. At page 18, line 19 and page 27, line 10, "Application Serial No. 09/796,259" should be updated to -- No. 6,554,511 --. Appropriate correction is required.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed. The following title is suggested: Parity Based Fault Tolerance Technique For A Memory System.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 6-8, 11, and 16-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Holland et al. further in view of Tuma et al. Holland et al. shows his system as a RAID, however, Tuma et al. teaches those skilled in the art at the time of applicants' invention that it is very desirable to use a solid state memory disk emulator instead of physical disk drives in order to significantly improve access time (see column 4, lines 16-44 of Tuma et al. for example), therefore, at the time of applicants' invention, it would have been obvious to one of ordinary skill in the art to substitute a solid state memory segment for each of the RAID disks of figures 1(a) and 1(b) of Holland et al. A comparison of Holland et al (as modified according to the teaching of Tuma et al.) with applicants' claims follows:

Applicants' claim 1	Holland et al.
A memory system, comprising: a plurality of memory boards	Figure 1 where DISK0 ...DISK4 would be implemented as memory board0 ...memory board4 in accordance with the teaching of Tuma et al.
each of the memory boards having a respective plurality of memory segments that may store respective data values	DISK0 through DISK4 would be implemented as solid state memories as taught by Tuma et al.
the segments being grouped into parity sets such that each of the parity sets includes respective segments of number N, the number N being an integer	In figure 1(b) D0.0, D0.1, D0.2, D0.3, P0 for example where N=5
the N respective segments in each respective parity set including a respective parity segment and N-1 respective data segments	N-1 data segments: D0.0, D0.1, D0.2, D0.3 parity segment: P0 for example
the N respective segments in each respective parity set being distributed among the memory boards such that none of the memory boards has more than one respective segment from each respective parity set	See figure 1(b): for example D0.0 is stored in DISK0 (memory board 0), D0.1 is stored in DISK1 (memory board 1) etc.
and a respective data value stored in a respective parity segment in at least one parity set may be calculated by a logical exclusive-or of respective data values stored in respective data segments in the at least one parity set	See the second equation in the left-hand column of page 423 of the reference: ($D_i.2 = D_i.0 \oplus D_i.1 \oplus P_i \oplus D_i.2$)

Tuma et al. make the limitations of claim 6 obvious to one of ordinary skill in the art at the time of applicants' invention as explained above.

Applicants' claim 7	Holland et al.
A memory system, comprising: a plurality of semiconductor memory segments;	Figure 1 where DISK0 ...DISK4 would be implemented as memory board0 ...memory board4 in accordance with the teaching of Tuma et al.
the segments being grouped into groups, each of the groups including N respective semiconductor memory segments, the number N being an integer	In figure 1(b) D0.0, D0.1, D0.2, D0.3, P0 for example where N=5
the N respective segments in each respective group comprising respective data segments and a respective parity segment	In figure 1(b) D0.0, D0.1, D0.2, D0.3, P0 for example where N=5
and in each of the groups: the respective parity segment stores a respective data value P that may be calculated by a logical exclusive-or of respective data values stored in the respective data segments	See the second equation in the left-hand column of page 423 of the reference: ($P_i = D_i.0 \oplus D_i.1 \oplus D_i.2 \oplus D_i.3$)

Applicants' claim 8	Holland et al.
The memory system of claim 7, wherein the plurality of memory segments are distributed among a plurality of electrical circuit boards such that none of the circuit boards includes more than one respective segment from each respective group	See figure 1(b): for example D0.0 is stored in DISK0 (memory board 0), D0.1 is stored in DISK1 (memory board 1) etc.

Applicants' claim 11	Holland et al.
A method of using a memory system, the memory system including a plurality of memory boards, each of the memory boards having a respective plurality of memory segments that may store respective data values,	Figure 1 where DISK0 ... DISK4 would be implemented as memory board0 ... memory board4 in accordance with the teaching of Tuma et al.
the method comprising: grouping the segments into parity sets such that each of the parity sets includes respective segments of number N, the number N being an integer	In figure 1(b) D0.0, D0.1, D0.2, D0.3, P0 for example where N=5
the N respective segments in each respective parity set including a respective parity segment and N-1 respective data segments,	N-1 data segments : D0.0, D0.1, D0.2, D0.3 parity segment: P0 for example
distributing the N respective segments in each respective parity set among the memory boards such that none of the memory boards has more than one respective segment from each respective parity set	See figure 1(b): for example D0.0 is stored in DISK0 (memory board 0), D0.1 is stored in DISK1 (memory board 1) etc.
and storing in a respective parity segment in at least one parity set a respective data value that may be calculated by logically exclusive-oring together respective data values stored in respective data segments in the at least one parity set.	See the first equation in the left-hand column of page 423 of the reference: ($Pi = Di.0 \oplus Di.1 \oplus Di.2 \oplus Di.3$)

Tuma et al. make the limitations of claim 16 obvious to one of ordinary skill in the art at the time of applicants' invention as explained above.

Applicants' claim 17	Holland et al.
A method of using a memory system, the system comprising a plurality of semiconductor memory segments	Figure 1 where DISK0 ...DISK4 would be implemented as memory board0 ...memory board4 in accordance with the teaching of Tuma et al.
the method comprising: grouping the segments into groups, each of the groups including N respective semiconductor memory segments, the number N being an integer	In figure 1(b) D0.0, D0.1, D0.2, D0.3, P0 for example where N=5
the N respective segments in each respective group comprising respective data segments and a respective parity segment	N-1 data segments: D0.0, D0.1, D0.2, D0.3 parity segment: P0 for example
and storing, in the respective parity segment in each of the groups, a respective data value P that may be calculated by logically exclusive-or-ing together respective data values stored in the respective data segments	See the first equation in the left-hand column of page 423 of the reference ($Pi=Di.0 \oplus Di.1 \oplus Di.2 \oplus Di.3$)

Applicants' claim 18	Holland et al.
The method of claim 17, wherein the method further comprises distributing the plurality of memory segments among a plurality of electrical circuit boards such that none of the circuit boards includes more than one respective segment from each respective group.	See figure 1(b): for example D0.0 is stored in DISK0 (memory board 0), D0.1 is stored in DISK1 (memory board 1) etc.

Claims 1-2, 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yashiro et al. further in view of Tuma et al. Yashiro et al. shows his system as a RAID, however, Tuma et al. teaches those skilled in the art at the time of applicants' invention that it is very desirable to use a solid state memory disk emulator instead of physical disk drives in order to significantly improve access time (see column 4, lines 16-44 of Tuma et al. for example), therefore, at the time of applicants' invention, it would have been obvious to one of ordinary skill in the art to substitute a solid state memory segment for each of the RAID disks of figures 1(a) and 1(b) of Yashiro et al. A comparison of Yashiro et al (as modified according to the teaching of Tuma et al.) with applicants' claims follows:

Applicants' claim 1	**Yashiro et al.**
A memory system, comprising: a plurality of memory boards	Figure 6 where Disks 32-1 ... 32-4 would be implemented as memory board0 ... memory board4 in accordance with the teaching of Tuma et al.
each of the memory boards having a respective plurality of memory segments that may store respective data values	Figure 6: Sectors 0 ... 3 of each disk as implemented in the form of memory boards.
the segments being grouped into parity sets such that each of the parity sets includes respective segments of number N, the number N being an integer	Figure 6: DATA a1 ... DATA c1 and PARITY P1
the N respective segments in each respective parity set including a respective parity segment and N-1 respective data segments	N-1 data segments : DATA a1, DATA b1, DATA c1 parity segment: P1 for example
the N respective segments in each respective parity set being distributed among the memory boards such that none of the memory boards has more than one respective segment from each respective parity set	See figure 6: for example DATA a1 is stored in DISK 32-1 (memory board 1), DATA b1 is stored in DISK 32-2 (memory board 2) etc.
and a respective data value stored in a respective parity segment in at least one parity set may be calculated by a logical exclusive-or of respective data values stored in respective data segments in the at least one parity set	Yashiro et al. teaches this by equations (5) and (6) near the top of column 15
Applicants' claim 2	**Yashiro et al.**
wherein: the number N is equal to 4	Yashiro et al shows, in figure 6 the case where N=4
Applicants' claim 4	**Yashiro et al.**
The memory system of claim 1, wherein: the number N is equal to 4	Yashiro et al shows, in figure 6 the case where N=4
a respective data value initially stored in one respective data segment in the at least one parity set is equal to variable value A, and a respective data value initially stored in the respective parity segment in the at least one parity set is equal to variable value P, the memory system includes circuitry that may be used to change the respective data values stored in the segments in the at least one parity set, and when the circuitry is used to change the one respective data value from the variable value A to another variable value A', the circuitry also changes the respective data value stored in the respective parity segment in the at least one parity set from a variable value P to another variable value P',the value P' being equal to P XOR A XOR A', where "XOR" represents a logical exclusive-or function.	From the two equations in column 22: substituting the first equation intermediate parity=A⊕A into the second equation yields P'=P⊕A⊕A

Applicants' claim 5	Yashiro et al.
The memory system of claim 4, wherein the circuitry is configured to change, in respective atomic operations, the one respective data value and the respective data value stored in the respective parity segment in the at least one parity set.	See column 23 lines 48-55: "At a time point when all of the new data, old data, and old parity are obtained, the exclusive OR is got in a lump by new data⊕old data⊕old parity=new parity (62) and the new parity is formed and the forming step of the intermediate parity can be also omitted."

Tuma et al. make the limitations of claim 6 obvious to one of ordinary skill in the art at the time of applicants' invention as explained above.

Applicants' claim 7	Yashiro et al.
A memory system, comprising: a plurality of semiconductor memory segments,	Figure 6 where Disks 32-1 ... 32-4 would be implemented as memory board0 ... memory board4 in accordance with the teaching of Tuma et al.
the segments being grouped into groups, each of the groups including N respective semiconductor memory segments, the number N being an integer	Tuma teaches to implement as semiconductor memory segments. In figure 6, Yashiro et al. teaches N=4 sectors.
the N respective segments in each respective group comprising respective data segments and a respective parity segment	N-1 data segments: DATA a1, DATA b1, DATA c1 parity segment: P1 for example
and in each of the groups: the respective parity segment stores a respective data value P that may be calculated by a logical exclusive-or of respective data values stored in the respective data segments	Yashiro et al. teaches this by equation (5) near the top of column 15 Old data D0⊕old data D1=old parity P0

Applicants' claim 8	Yashiro et al.
The memory system of claim 7, wherein the plurality of memory segments are distributed among a plurality of electrical circuit boards such that none of the circuit boards includes more than one respective segment from each respective group	See figure 6: for example DATA a1 is stored in DISK 32-1 (memory board 1), DATA b1 is stored in DISK 32-2 (memory board 2) etc.

Applicants' claim 9	Yashiro et al.
The memory system of claim 7, wherein: the number N is equal to 4;	Yashiro et al shows, in figure 6 the case where N=4
and in each of the groups: the value P stored in the respective parity segment is equal to A XOR B XOR C, where A, B, and C are respective data values stored in the respective data segments, where "XOR" represents a logical exclusive-or function	Yashiro et al. teaches this by equation (5) near the top of column 15

Applicants' claim 10	Yashiro et al.
The memory system of claim 7, further comprising: circuitry that may be used to implement an atomic operation by which one data value stored in one of the data segments in one of the groups may be changed from a first data value A to a second data value A', the circuitry also being usable to implement another atomic operation that changes to a data value P' the respective data value P stored in the respective parity segment in the one of the groups, the value P' being equal to P XOR A XOR A', where "XOR" represents a logical exclusive-or function.	From the two equations in column 22: substituting the first equation intermediate parity=A'⊕A into the second equation yields P'=P⊕A⊕A'

Applicants' claim 11	Yashiro et al.
A method of using a memory system, the memory system including a plurality of memory boards, each of the memory boards having a respective plurality of memory segments that may store respective data values,	Figure 6 where Disks 32-1 ... 32-4 would be implemented as memory board0 ... memory board4 in accordance with the teaching of Tuma et al.
the method comprising: grouping the segments into parity sets such that each of the parity sets includes respective segments of number N, the number N being an integer	Figure 6: Sectors 0 ... 3 of each disk as implemented in the form of memory boards.
the N respective segments in each respective parity set including a respective parity segment and N-1 respective data segments;	N-1 data segments : DATA a1, DATA b1, DATA c1 parity segment: P1 for example
distributing the N respective segments in each respective parity set among the memory boards such that none of the memory boards has more than one respective segment from each respective parity set	See figure 6: for example DATA a1 is stored in DISK 32-1 (memory board 1), DATA b1 is stored in DISK 32-2 (memory board 2) etc.
and storing in a respective parity segment in at least one parity set a respective data value that may be calculated by logically exclusive-or-ing together respective data values stored in respective data segments in the at least one parity set.	Yashiro et al. teaches this by equation (5) near the top of column 15

Applicants' claim 12	Yashiro et al.
The method of claim 11, wherein: the number N is equal to 4.	Yashiro et al shows, in figure 6 the case where N=4

Applicants' claim 14	Yashiro et al.
The method of claim 11, wherein: the number N is equal to 4.	Yashiro et al shows, in figure 6 the case where N=4
a respective data value initially stored in one respective data segment in the at least one parity set is equal to variable value A, and a respective data value initially stored in the respective parity segment in the at least one parity set is equal to variable value P; and the method further comprises: changing the one respective data value from the variable value A to another variable value A'; and changing the respective data value stored in the respective parity segment in the at least one parity set from a variable value P to another variable value P', the value P' being equal to P XOR A XOR A', where "XOR" represents a logical exclusive-or function.	From the two equations in column 22: substituting the first equation intermediate parity=A⊕A into the second equation yields P'=P⊕A'⊕A

Applicants' claim 15	Yashiro et al.
The method of claim 14, wherein the changing of the one respective data value and the changing of the respective data value stored in the respective parity segment in the at least one parity set are executed in atomic operations.	From the two equations in column 22: substituting the first equation intermediate parity=A⊕A into the second equation yields P'=P⊕A'⊕A

Tuma et al. make the limitations of claim 16 obvious to one of ordinary skill in the art at the time of applicants' invention as explained above.

Applicants' claim 17	Yashiro et al.
A method of using a memory system, the system comprising a plurality of semiconductor memory segments,	Figure 6 where Disks 32-1 ... 32-4 would be implemented as memory board0 ... memory board4 in accordance with the teaching of Tuma et al.
grouping the segments into groups, each of the groups including N respective semiconductor memory segments, the number N being an integer	Figure 6: Sectors 0 ... 3 of each disk as implemented in the form of memory boards.
the N respective segments in each respective group comprising respective data segments and a respective parity segment	Figure 6: DATA a1 ... DATA c1 and PARITY P1
and storing, in the respective parity segment in each of the groups, a respective data value P that may be calculated by logically exclusive-or-ing together respective data values stored in the respective data segments	Yashiro et al. teaches this by equation (5) near the top of column 15

Applicants' claim 18	Yashiro et al.
The method of claim 17, wherein the method further comprises distributing the plurality of memory segments among a plurality of electrical circuit boards such that none of the circuit boards includes more than one respective segment from each respective group.	See figure 6: for example DATA a1 is stored in DISK 32-1 (memory board 1), DATA b1 is stored in DISK 32-2 (memory board 2) etc.

Applicants' claim 19	Yashiro et al.
The method of claim 17, wherein: the number N is equal to 4;	Figure 6 shows the case where N=4
and in each of the groups, the value P stored in the respective parity segment is equal to A XOR B XOR C, where A, B, and C are respective data values stored in the respective data segments, where "XOR" represents a logical exclusive-or function.	Yashiro et al. teaches this by equation (5) near the top of column 15

Applicants' claim 20	Yashiro et al.
The method of claim 17, wherein the method further comprises: executing an atomic operation that causes one data value stored in one of the data segments in one of the groups to be changed from a first data value A to a second data value A', and also executing another atomic operation that changes to a data value P' the respective data value P stored in the respective parity segment in the one of the groups, the value P' being equal to P XOR A XOR A', where "XOR" represents a logical exclusive-or function.	See the equation at column 5, line 18-20 which is equivalent to $P'=A' \oplus A \oplus P$

Allowable Subject Matter

Claims 3 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Edirisooriya is cited to show a structure similar to that shown by Holland et al. and Yashiro et al. Ng et al. is cited to show uniformly distributing parity groupings throughout a storage array.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to R. Stephen Dildine whose telephone number is 703-305-5524. The examiner can normally be reached on M, Tu, Th, F 5:55 am to 4:25 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

R. Stephen Dildine

R. Stephen Dildine
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Art Unit 2133